Amendments to the Claims:

Re-write the claims as set forth below. This listing of claims will replace all prior versions and listings, of claims in the application:

Listing of Claims:

1.-23. (Canceled)

24. (Previously presented) A video graphics processing circuit comprises:

a processing unit; and

memory operably coupled to the processing unit, wherein the memory stores programming instructions that, when executed by processing unit, cause the processing unit to:

(a) receive display preferences regarding multiple displays;

(b) determine whether the display preferences can be fulfilled in observance of configuration properties of the multiple displays and configuration properties of a computing system, determine whether a current configuration of the multiple displays to the computing system can be reconfigured such that the display preferences corresponding to each of the multiple displays can be fulfilled while maintaining effective configuration of the current configuration when the display preferences cannot be fulfilled;

(c) configure the computing system and the multiple displays in accordance with the display preferences when the display preferences can be fulfilled, and reconfigure operable coupling of the multiple displays to the computing system such that the multiple displays are configured in accordance with the display preferences when the current configuration can be reconfigured;

(d) operably couple a display controller of the computing system to the multiple displays, the display controller simultaneously providing display data to the multiple displays;

(e) operably couple the display controller to a plurality of screen memories, each of the plurality of the screen memories storing separate display data and the display controller retrieving the display data from the plurality of screen memories; and

(f) operably couple the display controller to a plurality of display drivers, each of the plurality of display drivers writing the separate display data to the plurality of screen memories.

25.-28. (Canceled)

29. (Previously presented) The video graphics processing circuit of claim 24, wherein the memory further comprises programming instructions that cause the processing unit to operably couple a first display controller of the computing system to a first display of the at least one of the multiple displays and operably coupling a second display controller of the computing system to a second display of the multiple displays.

30. (Previously presented) The video graphics processing circuit of claim 29, wherein the memory further comprises programming instructions that cause the processing unit to operably couple the first display controller to a third display of the multiple displays.

31. (Previously presented) The video graphics processing circuit of claim 24, wherein the memory further comprises programming instructions that cause the processing unit to operably couple a first display controller of the computing system to a first display of the multiple displays, operably coupling a second display controller of the computing system to a second

display of the multiple displays, and operably coupling the first and second display controllers to one of the screen memory.

32. (Previously presented) The video graphics processing circuit of claim 31, wherein the memory further comprises programming instructions that cause the processing unit to operably couple at least two of the multiple displays to one of a plurality of screen memories.

33. (Previously presented) A digital storage medium for storing programming instructions that, when executed by a processing unit, cause the processing unit to configure multiple displays associated with a computing system, the digital storage medium comprises:

first means for storing programming instructions that cause a coupling controller of the processing unit to receive display preferences regarding the multiple displays;

second means for storing programming instructions that cause the coupling controller of the processing unit to determine whether the display preferences can be fulfilled in observance of configuration properties of the multiple displays and configuration properties of the computing system;

third means for storing programming instructions that cause the coupling controller of the processing unit to configure the computing system and the multiple displays in accordance with the display preferences when the display preferences can be fulfilled;

fourth means for storing programming instructions that cause the processing unit to:

determine whether a current configuration of the multiple displays to the computing system can be reconfigured such that the display preferences can be fulfilled while maintaining

effective configuration of the current configuration when the display preferences cannot be fulfilled;

reconfigure operable coupling of the multiple displays to the computing system such that the multiple displays are configured in accordance with the display preferences when the current configuration can be reconfigured;

operably couple a display controller of the computing system to the multiple displays, the display controller providing display data to the multiple displays;

operably couple the display controller to a plurality of screen memories, each of the plurality of the screen memories storing separate display data and the display controller simultaneously retrieving the display data from the plurality of screen memories; and

operably couple the display controller to a plurality of display drivers, each of the plurality of display drivers writing the separate display data to the plurality of screen memories.

34.-37. (Canceled)

38. (Previously presented) The digital storage medium of claim 33 further comprises means for storing programming instructions that cause the processing unit to operably couple a first display controller of the computing system to a first display of the multiple displays and operably coupling a second display controller of the computing system to a second display of the multiple displays.

39. (Previously presented) The digital storage medium of claim 38 further comprises means for storing programming instructions that cause the processing unit to operably couple the first display controller to a third display of the multiple displays.

40. (Previously presented) The digital storage medium of claim 33 further comprises means for storing programming instructions that cause the processing unit to operably couple a first display controller of the computing system to a first display of the multiple displays, operably coupling a second display controller of the computing system to a second display of the multiple displays, and operably coupling the first and second display controllers to a screen memory.

41. (Previously presented) The digital storage medium of claim 40 further comprises means for storing programming instructions that cause the processing unit to operably couple at least two of the multiple displays to one of a plurality of screen memories.

42. (Previously presented) A video graphics processing circuit for displaying at least one image on a plurality of displays, comprising:

a plurality of display controllers included on a single video graphics card;

a plurality of drivers;

memory, wherein at least a portion of the memory is screen memory, the screen memory having a plurality of screen memory portions, each of the plurality of screen memory portions storing separate display data;

coupling module operably coupled to a plurality of displays and the screen memory; and

a coupling controller operably coupled to receive display preferences and operative to determine whether the display preferences can be fulfilled in observance of configuration properties, the display preferences including at least one of displaying an image on more than one of the displays, displaying separate images on each of the displays, displaying a portion of the image on one of the displays and displaying the image on another one of the multiple displays, providing different refresh rates for at least two of the displays, providing different resolutions for at least two of the displays, selecting one of the displays to display a predetermined type of image, and displaying a first portion of the image on a first one of the displays and displaying a second portion of the image on a second one of the displays;

wherein, when the display preferences can be fulfilled, the coupling controller is operative to provide configuration requirements to the coupling module, wherein the coupling module, based on the configuration requirements, operably couples at least one of the plurality of display controllers with at least a portion of the screen memory and with at least one display, a respective display driver of the plurality of display drivers thereby writing respective separate display data to a respective one of the plurality of screen memory portions, and wherein the at least one of the plurality of display controllers retrieves display data from the at least a portion of the screen memory and simultaneously provides the display data to the plurality of displays, and wherein the coupling controller provides reconfiguration requirements to the coupling module when the display preferences cannot be fulfilled but a current configuration of the plurality of display controllers to the at least one display can be reconfigured such that the display preferences can be fulfilled while maintaining effective configuration of the current configuration.

43. (Previously presented) The video graphics processing circuit of claim 42 further comprises a graphics engine operably coupled, via the coupling module, to at least one of the plurality of display controllers and at least one of the display drivers.

44. (Previously presented) The video graphics processing circuit of claim 42 further comprises a user interface that is operably coupled to the coupling controller and to receive the display preferences from a user.

45. (Previously presented) The video graphics processing circuit of claim 42, wherein the memory further comprises properties memory that stores configuration properties of the plurality of display controllers and the at least one display, wherein the configuration properties include at least one of: limitations of the plurality of display controllers and the at least one display and operational rules of the plurality of display controllers and the at least one display.

46. (Previously presented) The video graphics processing circuit of claim 42, wherein the configuration requirements cause the coupling module to operably couple a first display controller of the plurality of display controllers to a first display and operably couple a second display controller of the plurality of display controllers to a second display.

47. (Previously presented) The video graphics processing circuit of claim 46, wherein the configuration requirements cause the coupling module to operably couple the first display controller to a third display.

48. (Previously presented) The video graphics processing circuit of claim 42, wherein the configuration requirements cause the coupling module to operably couple a first display controller of the plurality of display controllers to a first display, operably coupling a second display controller of the plurality of display controllers to a second display, and operably coupling the first and second display controllers to the screen memory.

49. (Previously presented) A video graphics processing apparatus for configuring a plurality of displays associated with a computer system, the apparatus comprising:

a common screen memory for multiple display controllers comprising a plurality of screen memory portions, each of the plurality of screen memory portions operative to store display data for the plurality of displays;

a plurality of display controllers included on a single video graphics card, each of the plurality of display controllers operative to retrieve display data from a screen memory portion of the common screen memory and simultaneously provide the display data to at least one respective display associated with a corresponding screen memory portion;

a plurality of display drivers operative to write the display data into the plurality of screen memory portions of the common screen memory;

a coupling module operative to couple to the plurality of display controllers, the plurality of display drivers, and the screen memory, the coupling module comprising means for switching the plurality of display drivers and the plurality of display controllers to appropriate screen memory portions; and

a coupling controller coupled to the coupling module, the coupling controller controlling, in response to configuration properties, operative to access to predetermined screen memory

portions by the plurality of display drivers, the coupling controller further operative to control, in response to the configuration properties, coupling of predetermined screen memory portions to the plurality of display controllers, wherein the configuration properties cause the coupling controller to couple a first display driver of the plurality of display drivers to a first and a second screen memory portion of the plurality of screen memory portions.

50. (Previously presented) The apparatus of claim 49 wherein the configuration properties cause the coupling controller to couple a first screen memory portion to more than one of the plurality of display controllers.

51. (Previously presented) The apparatus of claim 49 and further including a user interface coupled to the coupling controller, the user interface entering display preferences for the plurality of displays.

52. (Previously presented) The apparatus of claim 49 wherein the screen memory further comprises configuration memory that stores the configuration properties of the plurality of displays, the configuration properties including at least one of: display refresh rate, display resolution, and type of display.

53. (Previously presented) The apparatus of claim 49 wherein the configuration properties cause the coupling controller to couple a first display controller of the plurality of display controllers to a first and a second display of the plurality of displays.

54. (Canceled)

55. (Canceled)

56. (Previously presented) The apparatus of claim 49 wherein the plurality of display controllers simultaneously provide the display data to multiple displays.

57. (Previously presented) A video graphics processing circuit comprising:

a processing unit; and

memory operatively coupled to the processing unit, wherein the memory stores programming instructions that, when executed by the processing unit, cause a coupling controller of the processing unit to determine whether display preferences regarding multiple displays that display image information at the same time can be fulfilled in observance of configuration properties of the multiple displays and configuration properties of a computing system, and determine whether a current configuration of the multiple displays to the computing system can be reconfigured such that the display preferences can be fulfilled while maintaining effective configuration of a current configuration when the display preferences cannot be fulfilled.

58. (Currently amended) A method for configuring multiple displays comprising:

determining, in connection with an image or portion thereof to be displayed on the multiple displays at the same time, whether received display preferences can be fulfilled in observance of configuration properties of the multiple displays and configuration properties of a computing system;

determining whether a current configuration of the multiple displays to the computing system can be reconfigured such that the display preferences of the multiple displays can be fulfilled at the same time while maintaining effective configuration of a current configuration when the display preferences cannot be fulfilled; and

displaying the images [[of]]or a portion thereof on the multiple displays at the same time.

59. (Previously presented) The method of claim 58 comprising switching switches to couple differing screen memories with different display controllers to output display data to the multiple displays for simultaneous display.

60. (Previously presented) The video graphics processing circuit of claim 57 wherein the memory includes programming instructions that when executed by the processing unit, cause a coupling controller of the processing unit to reconfigure by dynamically connecting multiple display controllers to differing of the multiple displays for simultaneous display by the multiple displays.